Microprocessor 8086 objective questions answers pdf

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Here are 1000 MCQs on Microprocessor (Chapterwise). 1. What is Microprocessor? a) A multipurpose PLD that accepts binary data as input b) A multipurpose PLD that accepts an integer as input c) A multipurpose PLD that accepts whole numbers as input d) A multipurpose PLD that accepts prime numbers as input View AnswerAnswer: a Explanation: A microprocessor is a multipurpose PLD that accepts binary data as input and processes data according to the instructions, and outputs the result. Binary instructions are read from memory. 2. Which of the following is correct about 8086 microprocessor? a) Intel's first x86 processor b) Motrola's first x86 processor c) STMICROELECTRONICS's first x86 processor d) NanoXplore x86 processor View AnswerAnswer: a Explanation: The Intel 8086 is Intel's first x86 processor. They launched the most powerful processor in terms of advanced architecture i.e. 8086 processor in 1978. It has larger memory addressing capability and a powerful instruction set. 3. Which of the following is a type of microprocessor? a) CISC b) RISC c) EPIC d) All of the mentioned View AnswerAnswer: d Explanation: They are of three types: CISC: Complex Instruction Set Computer RISC: Reduced Instruction Set Computer EPIC: Explicitly Parallel Instruction Computing 4. The microprocessor of a computer can operate on any information if it is present in _____ only. a) Program Counter b) Flag c) Main Memory d) Secondary Memory View AnswerAnswer: c Explanation: If the information isn't in the computer's main store, the microprocessor can't do anything with it. The primary storage area in a computer, also known as main storage or memory, is where data is stored for easy access by the computer's processor. Random-access memory (RAM) and memory are frequently used interchangeably to refer to primary or main storage. 5. Which of the following technology was used by Intel to design its first 8-bit microprocessor? a) NMOS b) HMOS c) PMOS d) TTL View AnswerAnswer: c Explanation: PMOS technology was used for designing the processor because this technology was slow but simple. 6. Which of the following addressing method does the instruction, MOV AX,[BX] represent? a) register indirect addressing mode b) direct addressing mode c) register addressing mode d) register relative addressing mode View AnswerAnswer: a Explanation: In register indirect addressing mode the address of the operand is stored in the register. Since the instruction specifies that the register used to refer to the address is accessed indirectly, it represents the register indirect addressing mode. 7. What is the word length of an 8-bit microprocessor? a) 8-bits – 64 bits b) 4-bits – 32 bits c) 8-bits – 16 bits d) 8-bits – 32 bits View AnswerAnswer: a Explanation: At a time, an 8-bit CPU can process 8 bits of data. Depending on the type of microcomputer, the word length might range from 4 to 64 bits. 8. In 8-bit microprocessor, how many opcodes are present? a) 246 b) 278 c) 250 d) 256 View AnswerAnswer: a Explanation: In an 8-bit microprocessor, maximum 28 = 256 opcodes are possible. But it consists of only 246 opcodes. 9. Which of the following is not true about the address bus? a) It consists of control PIN 21 to 28 b) It is a bidirectional bus c) It is 16 bits in length d) Lower address bus lines (AD0 – AD7) are called "Line number" View AnswerAnswer: b Explanation: Data bus in the microprocessor is bidirectional but the address bus is unidirectional. AD0 – AD7 are the address lines that can be used for both address and data bus lines. 10. Which of the following is true about microprocessors? a) It has an internal memory b) It has interfacing circuits c) It contains ALU, CU, and registers d) It uses Harvard architecture View AnswerAnswer: c Explanation: Microprocessors don't have memory and interfacing circuits. They follow Princeton architecture and they contain ALU, CU, and registers inside them. 11. Which of the following is the correct sequence of operations in a microprocessor? a) Opcode fetch, memory read, memory write, I/O read, I/O write b) Opcode fetch, memory write, memory read, I/O read, I/O write c) I/O read, opcode fetch, memory read, memory write, I/O write d) I/O read, opcode fetch, memory write, memory read, I/O write View AnswerAnswer: a Explanation: Initially, the opcode is fetched from memory, then memory read and write operations are performed followed by I/O read and I/O write operations. 12. The _____ directive instructs the assembler to begin memory allocation for a segment/block/code from the stated address. a) GROUP b) OFFSET c) ORG d) LABEL View AnswerAnswer: c Explanation: When an ORG is written, the assembler starts the location counter to keep track of the module's allotted address as specified in the directive. The location counter is initialized to 0000H if the directive is not present. 13. Which of the following is not a microprocessor? a) Z8000 b) Motorola 6809 c) Zilog Z8 d) PIC1x View AnswerAnswer: d Explanation: Z8000, Motorola 6809, and Zilog Z8 are microprocessors but PIC1x is an 8-bit microcontroller. 14. Which of the following is not a property of TRAP interrupt in microprocessor? a) It is a non-maskable interrupt b) It is of highest priority c) It uses edge-triggered signal d) It is a vectored interrupt View AnswerAnswer: c Explanation: TRAP interrupt in 8085 microprocessor uses both level and edge-triggered clock because it is of highest priority among all the interrupts. 15. Which of the following is a property of RST 7.5 interrupt? a) It is a non-maskable interrupt b) It has 3rd highest priority c) It uses level-triggered signal d) Its vectored address is 003C H View AnswerAnswer: d Explanation: RST 7.5 is a maskable interrupt with 2nd highest priority after RST-4.5. It uses only the edge-triggered signal. It is a vectored interrupt and its vectored address is 003C H. 16. Which of the following flag is used to mask INTR interrupt? a) zero flag b) auxiliary carry flag flag c) interrupt flag d) sign flag View AnswerAnswer: c Explanation: If the interrupt flag, IF=1, is set, the microprocessor will serve any interrupt. The processor ignores the service if the interrupt flag, IF=0, is set to 0. 17. Which of the following is a special-purpose register of microprocessor? a) Program counter b) Instruction register c) Accumulator d) Temporary register View AnswerAnswer: a Explanation: Instruction register, accumulator, and temporary register are general-purpose registers but program counter is a special-purpose register because it holds the address of the next instruction. 18. Which of the following circuit is used as a special signal to demultiplex the address bus and data bus? a) Priority Encoder b) Decoder c) Address Latch Enable d) Demultiplexer View AnswerAnswer: c Explanation: Address Latch Enable is a positive pulse and it is generated whenever the microprocessor starts an operation to latch the lower order address lines (AD7 to AD0). 19. How many flip-flops are there in a flag register of 8085 microprocessor? a) 4 b) 5 c) 7 d) 10 View AnswerAnswer: b Explanation: There are five flags or flip-flops in a flag register in 8085 microprocessor that shows the status after ALU operation. They are mainly affected by the content of the accumulator. 20. Which of the following flag condition is used for BCD arithmetic operations in microprocessor? a) Sign flag b) Auxiliary carry flag c) Parity flag d) Zero flag View AnswerAnswer: b Explanation: Among all the five flag conditions in microprocessor, the auxiliary carry flag is used internally for BCD arithmetic operations. Based on the auxiliary flag, the instruction set doesn't contain the conditional jump operation. 21. Whenever a non-maskable interrupt occurs in 8085 microprocessor, which of the following data line contains the data? a) 2C H b) 3C H c) 36 H d) 24 H View AnswerAnswer: d Explanation: TRAP interrupt is a non-maskable interrupt with the highest priority. When it occurs, its vectored address 0024 H is placed on the program counter. 24 H is the lower address bus which also acts as the data bus. 22. What does a microprocessor understand after decoding opcode? a) Perform ALU operation b) Go to memory c) Length of the instruction and number of operations d) Go to the output device View AnswerAnswer: c Explanation: After decoding the opcode of the instruction, a microprocessor understands the length of the instruction and the total number of operations to be performed. 23. How many address lines are present in 8086 microprocessor? a) 16 b) 20 c) 32 d) 40 View AnswerAnswer: b Explanation: 8086 microprocessor is a 16-bit microprocessor that uses 20 address lines and 16 data lines. AD0 to AD15 are 16 lower order address lines that can be operated in both address and data bus mode. 24. Which of the following is not a status flag in microprocessor? a) Overflow flag b) Direction flag c) Interrupt flag d) Index flag View AnswerAnswer: d Explanation: Overflow flag represents whether the result is out of scope or not. Direction flag is used in string operations and interrupt flag is used to enable the interrupts. 25. Which of the following is not a condition flag? a) Trap flag b) Auxiliary carry flag c) Parity flag d) Zero flag View AnswerAnswer: a Explanation: Trap, direction, and interrupt are the control flags. Carry, parity, auxiliary carry, zero, sign and overflow flags are the condition flags. 26. Which of the following register is not used in opcode fetch operations? a) Program counter b) Memory address register c) Memory data register d) Flag register View AnswerAnswer: d Explanation: Flag register is not used in opcode fetch operations. It is used to represent the status of ALU operation which is performed after decoding of the opcode. 27. A memory connected to a microprocessor has 20 address lines and 16 data lines. What will be the memory capacity? a) 8 KB b) 2 MB c) 16 MB d) 64 KB View AnswerAnswer: b Explanation: Total number of locations of the memory possible for 20 address lines is 220 and every location has 16/8 = 2 bytes. So, total memory capacity will be 220 × 2 = 2 MB. 28. What is the word length of the Pentium-II microprocessor? a) 8-bit b) 32-bit c) 64-bit d) 16-bit View AnswerAnswer: c Explanation: The Pentium-II microprocessor is a 64-bit microprocessor. It was introduced in 1997 and designed with 7.5 million transistors. Its word length is 64-bit. 29. Which of the following is not true about 8085 microprocessor? a) It is an 8-bit microprocessor b) It is a 40 pin DIP chip c) It is manufactured using PMOS technology d) It has 16 address lines View AnswerAnswer: c Explanation: 8085 microprocessor is manufactured using NMOS technology. PMOS technology is used in a 4004 microprocessors. NMOS technology is faster than PMOS technology. 30. Which of the following is a non-vectored input? a) TRAP b) RST-7.5 c) RST-6.5 d) INTR View AnswerAnswer: d Explanation: TRAP, RST-7.5, and RST-6.5 are vectored inputs but INTR is a non-vectored input. It has the least priority and its address is provided by the user using an external device. 31. Which of the following is true? a) Every instruction has two parts i.e. opcode and operands b) MOV B, C is a two-byte instruction c) MVI A, 90H is a three-byte instruction d) Maximum number of T-states possible for the execution of an instruction is 16 View AnswerAnswer: a Explanation: MOV B, C is a one-byte instruction. MVI A, 90H is a two-byte instruction and the maximum number of T-states possible for the execution of an instruction in 8085 microprocessor is 18. 32. Which of the following addressing mode is used by 8085 microprocessor for array and list operations? a) Base-Register b) Direst c) Indexed d) Immediate View AnswerAnswer: c Explanation: Indexed addressing mode is used for array and list operations. It uses a constant value and index register to execute the instruction. 33. What is stored in the H & L general-purpose register? a) Opcode b) Address of memory c) Address of next instruction d) Temporary data View AnswerAnswer: b Explanation: H and L are 8-bit general-purpose registers. They are used to store the address of memory. Together they can store a 16-bit address. 34. If a 90 GB memory has to be connected to a microprocessor, minimum how many address lines are required? a) 36 b) 39 c) 32 d) 37 View AnswerAnswer: d Explanation: 90 GB is greater than 64 GB and less than 128 GB. For 64 GB (236 Bytes), a minimum of 36 address lines are needed. So, for 90 GB, we need 36 + 1 = 37 address lines. 35. Which of the following is a software interrupt? a) TRAP b) INTR c) RST-6.5 d) RST-5 View AnswerAnswer: d Explanation: TRAP, INTR, and RST-6.5 are the hardware interrupts but RST-5 is a software interrupt present. All software interrupts are vectored interrupts. 36. What is the vectored address of RST-5? a) 0010 H b) 0032 H c) 0028 H d) 0030 H View AnswerAnswer: c Explanation: Vectored address of RST-n is calculated by the formula n × 8. So, vectored address of RST-5 is (40)10. (40)10 in hexadecimal is (28)16 = 0028 H. 37. Which of the following is true about stack pointer? a) Stack pointer contains the address of the top of the stack memory b) Stack pointer is an 8-bit register c) Stack pointer stores data permanently d) Stack pointer is initialized after stack operation View AnswerAnswer: a Explanation: Stack pointer is initialized before stack operation, it is a 16-bit register that stores data temporarily. It follows a LIFO operation. So, it contains the address of the top of the stack memory. 38. How many address lines are required to connect a 4 KB RAM to a microprocessor? a) 10 b) 16 c) 12 d) 20 View AnswerAnswer: c Explanation: 4 KB RAM is equal to 4096 × 8 bits. Total number locations are (4096 × 8)/8 = 4096 and 4096 = 212. So, 12 address lines are required to connect a 4 KB RAM to a microprocessor. 39. Which of the following is true about MOV A, B instruction? a) It means move the content of register A to register B b) It uses immediate addressing mode c) It doesn't affect the flag register d) It is a 2-byte instruction View AnswerAnswer: c Explanation: MOV A, B means moving the content of register B to register A. It is a 1-byte instruction and it uses register addressing mode. No flags are affected because operations of this instruction are not performed in the ALU. 40. Which of the following is false about LDA instruction? a) It is a 3-byte instruction b) It uses indirect addressing mode c) It has 13 T-states d) It doesn't affect any flags View AnswerAnswer: b Explanation: LDA is a direct addressing mode instruction which stands for Load Accumulator Direct. It is a 3-byte instruction and it has 13 T-states. No flags are affected by this instruction. 41. Which is of the following is true about STA instruction? a) It uses immediate addressing mode b) It is a 3-byte instruction c) It required three machine cycles d) Accumulator is loaded with the content of memory View AnswerAnswer: b Explanation: STA is a direct addressing mode instruction which stands for Store Accumulator Direct. It is a 3-byte instruction and it requires four machine cycles. In STA instruction memory is loaded with the content of the accumulator. 42. DAA instruction is used to perform which type of addition? a) BCD addition b) Excess-3 addition c) Binary addition d) Octal addition View AnswerAnswer: a Explanation: DAA instruction is used to perform BCD addition. DAA instruction changes the binary values of the contents of the accumulator to BCD. 43. What does a loader do in a microprocessor? a) Converts hexadecimal code to binary b) Converts decimal to binary c) Increments the content of the program counter by 1 d) Decodes an opcode View AnswerAnswer: a Explanation: Microprocessor understands only 0s & 1s. So, a loader first converts hexadecimal code to binary form and then loads it to the memory. 44. Suppose registers 'A' and 'B' contain 50H and 40H respectively. After instruction MOV A, B, what will be the contents of registers A and B? a) 40H, 40H b) 50H, 40H c) 50H, 50H d) 60H, 40H View AnswerAnswer: a Explanation: Initially, register A contains 50H & B contains 40H. Instruction MOV A, B means move the content of B to A. So, after this operation, both registers A & B will contain 40H. 45. For how many times per instruction, the content of the program counter is placed on the address bus? a) One time b) Two times c) Depends on the memory capacity of the processor d) Depends on the length of the instruction View AnswerAnswer: d Explanation: After decoding an opcode the microprocessor understands the length of the instruction. So, the content of the program counter is placed on the address bus as many times as the length of the instruction. 46. Conditional instructions are independent of which of the following flag? a) Z b) AC c) CY d) P View AnswerAnswer: b Explanation: Conditional instructions are the branching instructions. In this group, the program control is transferred from one location to another conditionally. They depend on the status of flags affected for previous ALU operations accept the AC flag. 47. Which of the following is not correct about HLT instruction? a) It is a machine control instruction b) It is used to start the execution of the program c) PC is disconnected from the address bus d) A reset interrupt is required to come out of halt state View AnswerAnswer: b Explanation: HLT is a machine control statement. Internally, the PC is disconnected from the address bus so, the next fetch is not possible. It is used mainly to stop the execution of the program. 48. When data required for instruction is present inside the register of a microprocessor then which of the following addressing mode is used? a) Indexed b) Register c) Relative d) Direct View AnswerAnswer: b Explanation: Register addressing mode is used when data is present inside the register of the microprocessor. For example, MOV B, C. Here, B and C are the registers of the microprocessor. 49. Which of the following interfacing IC is a DMA controller? a) 8257/37 b) 8155 c) 8253/54 d) 8279 View AnswerAnswer: a Explanation: 8155 is a multipurpose programmable I/O device. 8253/54 is a programmable counter. 8279 is a keyboard/display controller and 8257/37 is a DMA controller. 50. Which of the following is a 2-word instruction set? a) LDA 2500H b) MOV A, B c) IN 01H d) JMP 2085H View AnswerAnswer: c Explanation: LDA 2500H and JMP 2085H are 3-word instructions. MOV A, B is a 1-word instruction. IN 01H is a 2-word instruction, the first byte specifies the opcode and the second byte specifies the operand. 51. Which of the following is a register-indirect addressing mode instruction set? a) LDA 2700H b) ADI 36H c) DAA d) LDAX B View AnswerAnswer: d Explanation: LDA 2700H is a direct addressing mode instruction. ADI 36H is an immediate addressing mode instruction. DAA is an implicit addressing mode and LDAX B is a register-indirect addressing mode instruction. 52. Which is of the following is true about SPHL instruction? a) It uses indexed addressing mode b) It is a 3-byte instruction c) It requires three T-states d) Contents of HL pair is moved to SP View AnswerAnswer: d Explanation: SPHL is a 1-byte instruction. It uses register addressing mode. It required 6 T-states and it means moving the contents of the HL pair to SP. Our 1000+ MCQs focus on all topics of the Microprocessor subject, covering 100+ topics. This will help you to prepare for exams, contests, online tests, quizzes, viva-voce, interviews, and certifications. You can practice these MCQs chapter by chapter starting from the 1st chapter or you can jump to any chapter of your choice. You can also download the PDF of Microprocessor MCQs by applying below. If you would like to learn "Microprocessor" thoroughly, you should attempt to work on the complete set of 1000+ MCQs - multiple choice questions and answers mentioned above. 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